HYBRID PHASE/DELAY LOCKED LOOP CIRCUITS AND METHODS

ABSTRACT OF THE DISCLOSURE

[0068] A circuit is provided that aligns the phase of a delay signal with an input clock signal. The circuit functions as a phase locked loop (PLL) in a first state of operation and as a delay locked loop (DLL) in a second state of operation. An adjustable delay circuit generates the delay signal. A phase detector compares the input clock signal to the delay signal to generate a phase detection signal. The adjustable delay circuit adjusts the phase of the delay signal in response to the phase detection signal. A multiplexer couples the delay signal back to the input of the adjustable delay circuit using a feedback loop in the first state of operation. The multiplexer couples the input clock signal to the input of the adjustable delay circuit in the second state of operation.